WHAT IS CLAIMED IS:

- 1. A semiconductor device including
- a variable capacitor, the variable capacitor comprising
- a first semiconductor layer of a first conductivity type,
- 5 and
 - a second semiconductor layer epitaxially grown on the first semiconductor layer,

wherein a PN junction region serving as a variable capacitance is formed at a boundary between the first semiconductor layer and the second semiconductor layer.

- The semiconductor device according to claim 1, further including a bipolar transistor having
 - a third semiconductor layer, and
- a fourth semiconductor layer epitaxially grown on the third semiconductor layer,

wherein the fourth semiconductor layer has a base layer epitaxially grown simultaneously with the second semiconductor layer.

20

3. The semiconductor device according to claim 1, wherein the first semiconductor layer is a Si layer, and the second semiconductor layer is a $Si_{1-x-y}Ge_xC_y$ layer (0 < x < 1, 0 . y < 1).

- 4. The semiconductor device according to claim 1, further including an oscillation circuit, wherein the variable capacitor is connected to the oscillation circuit.
- 5. A method for manufacturing a semiconductor device including a variable capacitor and a bipolar transistor on a common semiconductor substrate, comprising the steps of:

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- (a) forming a first semiconductor layer of a first conductivity type in a region of the semiconductor substrate where the variable capacitor is to be formed, and forming a second semiconductor layer of the first conductivity type in a region of the semiconductor substrate where the bipolar transistor is to be formed; and
- (b) after the step (a), forming a third semiconductor
 15 layer on the first semiconductor layer of the semiconductor
 substrate and forming a fourth semiconductor layer on the
 second semiconductor layer both by an epitaxial growth method.
- 6. The method according to claim 5, wherein a collector diffusion layer of the bipolar transistor is formed in the step (a), and a base layer of the bipolar transistor is formed in the step (b).
- 7. The method according to claim 5 or 6, wherein the third and fourth semiconductor layers each including a Si_{1-x-}

 $_{y}Ge_{x}C_{y}$ layer (0 < x < 1, 0 . y < 1) are formed in the step (b).